Epitaxial Growth I

Effect of the Si Droplet Size on the VLS Growth Mechanism of SiC Homoepitaxial Layers
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Homoepitaxial "Web Growth" of SiC to Terminate C-Axis Screw Dislocations and Enlarge Step-Free Surfaces
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3C-SiC(100) Homoepitaxial Growth by Chemical Vapor Deposition and Schottky Barrier Junction Characteristics
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Void-free Epitaxial Growth of Cubic SiC Crystallites during CO Heat Treatment of Oxidized Silicon
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Heteroepitaxy of Cubic SiC on Si(100) Using Porous Si as a Compliant Seed Crystal
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Effect of the Si droplet size on the VLS growth mechanism of SiC homoepitaxial layers

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For some applications as electrical power conditioning and distribution, thick (several tens of μm) active drift SiC epilayers are required. Until now, only high temperature processes (> 1700°C) such as sublimation sandwich method, liquid phase epitaxy (LPE) and high temperature CVD are able to provide high growth rates suited for thick layer deposition. Vapour-Liquid-Solid (VLS) mechanism has demonstrated as high growth rate as several mm/h at 1100°C for SiC whiskers [1]. The transposition of such a mechanism to SiC epilayer growth would combine the advantages of the CVD technique (growth control) with the ones of the LPE technique (low supersaturation). However, the main problem to solve is the increase of the droplet size from few micrometers for the whiskers to the whole SiC wafer size. A promising attempt in this way was already made by A. Leycuras in a specially design reactor [2].

Experiments were carried out in a conventional vertical cold wall CVD reactor working at atmospheric pressure with SiH_4 and C_3H_8 as reactants and H_2 or Ar as vector gases. 3C-SiC epilayer grown on Si(100) and 8° off misoriented 4H-SiC (0001) crystals were used as substrates. Liquid silicon was chosen as the catalyst for the VLS mechanism. Temperatures ranged from 1500°C to 1700°C. We can separate our investigations in two configurations : 1) pieces of Si wafers as Si source were placed on top of the SiC seeds, and only propane was used as reactant; 2) CVD like conditions were used with a high excess of silane compared to propane (C/Si<1).

In the first configuration, a single and big droplet (few mm diameter and height) formed whereas a set of small droplets (several tens of μm diameter and height) formed on the entire surface in the second configuration. The size of the liquid droplet plays an important role on the VLS mechanism. Indeed, if the droplet is too big, it cannot be assumed as isothermal. This is the case in the first configuration where the VL interface should be enough cooler than the LS interface so that the liquid can dissolve less carbon at its free surface than at the LS interface. So the thermal gradient inside the droplet is opposed to the carbon activity gradient required for crystal growth at the SiC surface. However, due to the propane flux inside the chamber, a forced supersaturation regime is set inside the droplet giving rise to effective growth at the SiC surface. It was found that the growth rate increases and the morphology worsen from the center to the edge of the droplet. With the second configuration (several small droplets), the growth rate is homogeneous on the whole surface even if the morphology shows a more step-bunched structure under the droplets than outside. Proof will be given that a VLS mechanism occurred with this second configuration and uniform growth rates up to 35 μm/h at 1600°C were demonstrated.

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Hetero-epitaxial growth and characteristics of 3C-SiC on large-diameter Si(001) substrate

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A novel technique that eliminates planar defects in 3C-SiC hetero-epitaxial layer on Si(001) substrate was developed. Planar defects generated at an interface between 3C-SiC and Si substrate can be classified into two types: anti-phase boundaries (APBs) and twin boundaries (TBs). Although it is well known that step flow epitaxy of 3C-SiC on a slightly misoriented Si(001) substrate in the [110] direction (off-Si) result in elimination of APBs, TBs hardly be eliminated. This is because TBs are arranged in parallel with only (111) plane, with reduced possibility of elimination through combination with countered TBs with increasing 3C-SiC thickness. Therefore, TBs must be arranged in parallel, not only with the (111) plane, but with the $(\bar{1}11)$ plane equaling statistical ratio, to realize effective TB elimination at the intersection of two TBs. To satisfy above condition, Si(001) surface with countered slopes oriented in the [110] and $[\bar{1}10]$ directions (undulant-Si) was thought to be an effective substrate for 3C-SiC epitaxial growth.

To confirm above effects of the undulant-Si substrate, the entire surface of 6 inches Si(001) substrate was scraped by diamond slurry toward the $[\bar{1}10]$ direction to form continuous undulations, the ridges of which were arranged along the $[\bar{1}10]$ direction. Then the 3C-SiC layer was grown on undulant-Si substrate using 50 sccm of SiH_2Cl_2 as a Si source and 10 sccm of C_2H_2 as a C source, with 100 sccm of H_2 as a carrier gas at 1350 ° C. An epitaxial 3C-SiC layer of about 200 μm in thickness was obtained on the undulant-Si substrate via five hours growth process.

3C-SiC epitaxial layer grown on undulant-Si exhibited a mirror-like surface even after etching by molten KOH unlike that case on off-Si. It appears that the undulant-Si eliminated with remarkable success not only APBs, but TBs, through the following mechanism. At first, the APBs generated at the initial stage of 3C-SiC growth were eliminated at each slope on undulant-Si by the same mechanism found on the off-Si. Although TBs remained in the 3C-SiC layer even after all

APBs had been eliminated, these were arranged in parallel along the (111) plane or the ($\bar{1}\bar{1}1$) plane, forming countered steps, as shown in Fig.1a). Thus, TB density, that is density of steps, on the surface of 3C-SiC grown on undulant-Si would decrease with increasing 3C-SiC thickness, through the combination of TBs which countered, as shown in Fig.1 b) and c). The most significant aspect of 3C-SiC growth on an undulant-Si substrate is that the vanishing probability of ($\bar{1}\bar{1}1$) paralleled TBs was quite similar to that of (111) paralleled TBs.

The crystallinity and electric properties of 3C-SiC grown on undulant-Si will be discussed at the conference using results of XTEM observation, x-ray diffraction, RBS, and Hall effect.

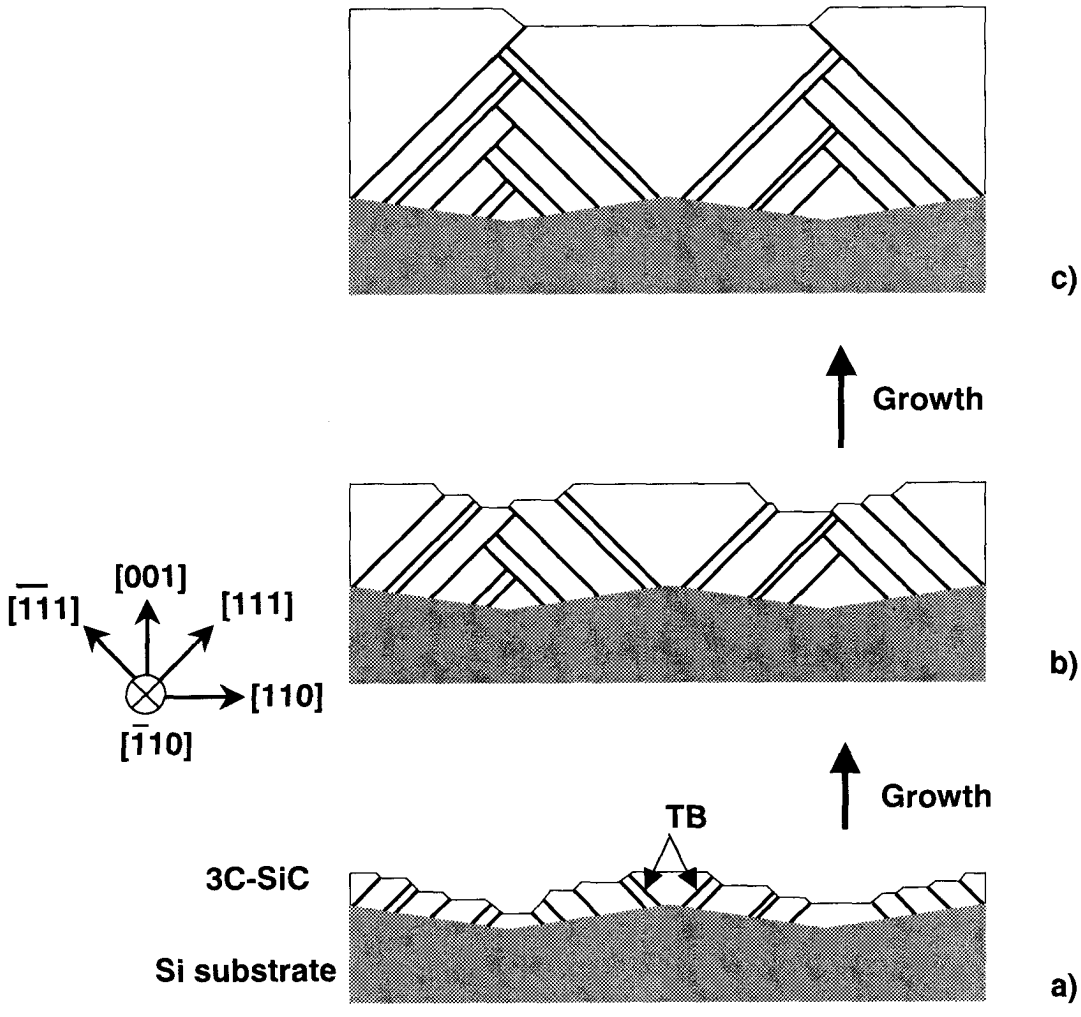

Fig.1 Vanishing model of TBs in 3C-SiC layer on undulant-Si: The ($\bar{1}$10) cross-sectional structure of 3C-SiC changes from a) to b) and c) as 3C-SiC growth progresses.

Homoepitaxial "Web Growth" of SiC to Terminate C-Axis Screw Dislocations and Enlarge Step-Free Surfaces

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Abstract

Homoepitaxial CVD growth of thin lateral cantilevers emanating from the edges of mesa patterns that were dry-etched into on-axis commercial 4H-SiC substrates prior to growth is reported. Cantilevers on the order of a micrometer thick extending tens of micrometers from the edge of a mesa have been grown. The termination of vertically propagating screw dislocations, including a micropipe, that are overgrown by the cantilevers has been demonstrated, in large part because the crystal structure of the cantilevers is established laterally from the mesa sidewalls. The cantilevers form in epitaxial growth conditions where the two-dimensional terrace nucleation rate is close enough to zero that device-size mesa top surfaces (as large as 0.4 x 0.4 mm observed to date) become entirely step free as previously described [1]. After stepflow growth removes almost all atomic steps from the top surface of a mesa, additional adatoms collected by the large stepfree surface diffuse to the mesa sidewall to find steps where they rapidly incorporate into the crystal near the top of the mesa sidewall. The lateral propagation of the step-free cantilevered surface is significantly affected by pregrowth mesa shape and orientation, with the highest lateral expansion rates being observed at the inside concave corners of V-shaped pre-growth mesas. The cantilevers exhibit well-known hexagonal crystal growth facets, with fastest growth observed along the $<11\bar{2}0>$ direction. Complete spanning of the interiors of V's and other mesa shapes with concave corners by "webbed cantilevers" is accomplished. Webbed cantilever surfaces up to approximately 0.4 x 0.7 mm have been realized to date, representing a 4-fold increase from the pre-growth mesa area. X-ray topography and AFM analysis of webbed regions formed over screw dislocations indicate that c-axis propagation of these defects is terminated. With very few exceptions, cantilevers are not observed on mesas that contain screw dislocations prior to epitaxial growth, as the screw dislocations readily provide steps for incorporating top surface adatoms into the crystal resulting in vertical growth of the mesa top surface [1]. Another factor observed to limit lateral cantilever growth is unintentional two-dimensional nucleation and growth of 3C-SiC that takes place on some mesa/cantilever surfaces.

[1] J. A. Powell, et. al., Appl. Phys. Lett., 77(10), p. 1449 (2000).

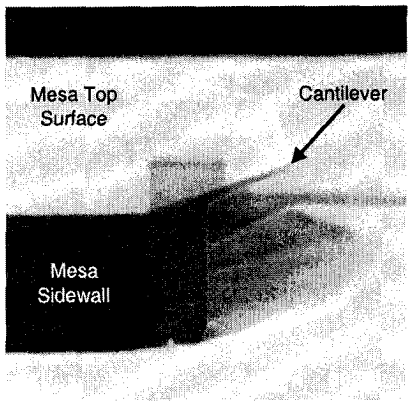


Fig. 1: SEM of thin lateral 4H-SiC cantilever emanating from the top of a flat mesa.

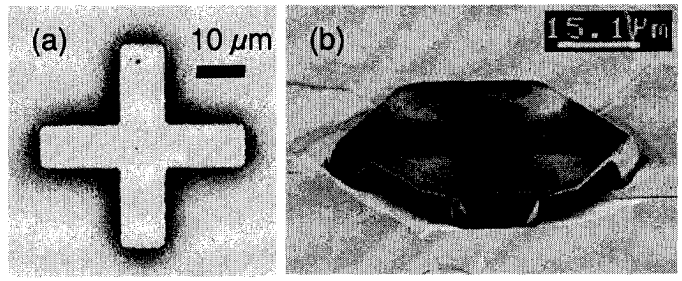
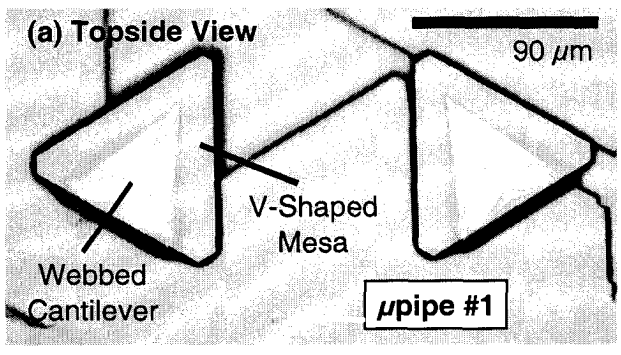


Fig. 2: (a) Pre-growth optical photo of cross-shaped mesa. **(b)** Post-growth SEM of step-free "webbing" formed by ordered merging of lateral cantilevers following 1-hour growth.



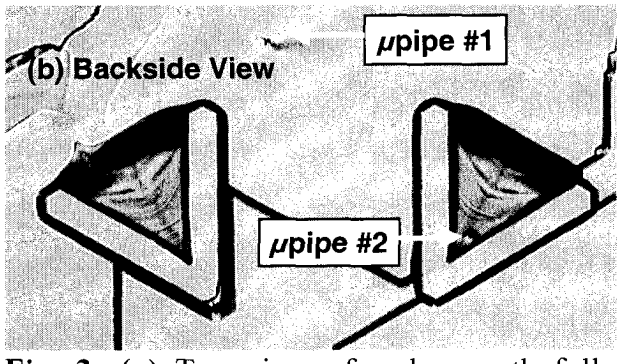
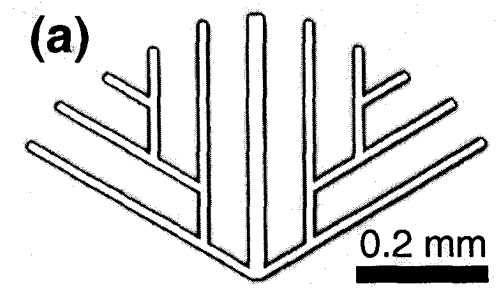


Fig. 3: (a) Top view of web growth fully spanning two V-shaped mesas following a 6-hour epitaxial growth. AFM scans of the right mesa did not detect the presence of any atomic steps, confirming that micropipe #2 did not propagate through the webbing. The presence of a few 0.25 nm steps was detected on the left mesa, indicating unintentional nucleation and growth of 3C-SiC on that particular mesa.
(b) View of the same mesas looking through the polished wafer backside, showing micropipe #2 beneath the webbing.



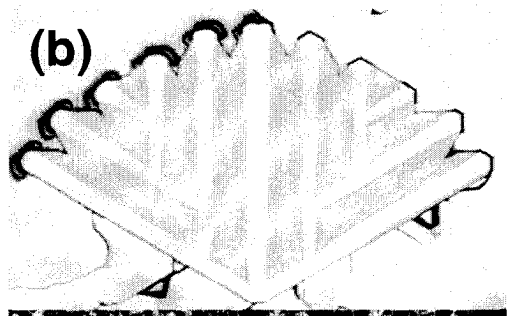


Fig. 4: (a) Pre-growth and **(b)** post-growth optical photo of large web growth test mesa. The webbing process increased the top surface area by over a factor of 4 following the 6-hour growth.
(c) X-ray back-reflection topograph used to study the defect microstructure around the post-growth mesa.

3C-SiC(100) Homoepitaxial Growth by Chemical Vapor Deposition and Schottky Barrier Junction Characteristics

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We have investigated 3C-SiC heteroepitaxial growth on Si using chemical vapor deposition method (CVD) and found out that atomically flat surfaces without protrusions and antiphase domain (APD) are obtained by using low pressure CVD (LPCVD) [1, 2]. And we have showed excellent Schottky barrier junction (SBJ) properties using the LPCVD epilayers compared with those reported for 3C-SiC on Si so far. However, the characteristics of the SBJ, like breakdown voltage and reverse leakage current, were not sufficient for practical use [3]. These poor characteristics have been attributed to the low crystallinity of the epilayers, namely the epilayers contain many defects such as stacking faults and twins. In the case of the growth of 3C-SiC on Si substrates, the growth temperature is limited by the melting point of Si, i.e., 1420 ℃. Therefore, it is difficult to improve the crystallinity by increasing growth temperatures. Recently, thick 3C-SiC free standing crystals, around 200 μm in thickness, were made by removing Si substrates from thick 3C-SiC heteroepitaxial layers [4]. In this report, we have used 3C-SiC free standing crystals as substrates and have carried out the 3C-SiC homoepitaxial growth. We have examined their crystallinity by studying the characteristics of the Schottky barrier junction fabricated on them.

The homoepitaxial growth of 3C-SiC were carried out by use of low pressure hot-wall reactor CVD system. The 3C-SiC substrates with on-axis (100) surfaces, n type with carrier concentrations of 1×10^{17} cm^{-3} and the thickness of about 200 μm were supplied by HOYA corporation [5]. We have grown SiC epilayers, 10 μm in thickness, with various growth conditions, *i.e.*, pressures between 90 and 300 Torr, Si/C ratio between 0.33 and 1 and growth temperatures between 1500 and 1600 ℃. The epilayers was examined with a Nomarski differential interference contrast microscopy (NDIC), an atomic force microscope (AFM) and X-ray diffraction (XRD). Schottky diodes were fabricated on these epilayers. Details of the process have been described elsewhere [3]. Ni films were deposited as Schottky electrodes and Al ohmic electrodes were formed on back side of the substrates. The diameter of the Schottky electrodes was 0.1 mm.

Figure 1 shows a NDIC image of the surfaces of homo-epilayers. Smooth surfaces on which any features could not be observed, as shown in Fig. 1, were obtained at the optimized conditions. Figure 2 shows an AFM image of a sample with smooth surface. The figure shows that the step bunching occurs. The width of the terrace is about 5 μm and the step height is 1-3 nm. The average roughness (16 μm square) was 0.85 nm, which is one order of magnitude smaller than those of hetero-epilayers reported. The full width at half maximum (FWHM) of the X-ray rocking curve for (400) peak were in the range from 163 to 484 arcsec. We could not find any relation between the value of FWHM and the growth conditions, because the variation of the FWHM values of substrates is larger than the difference of those

by the growth conditions. An example of the I-V characteristic of a Ni/n-type 3C-SiC Schottky diode is shown in Fig. 3. The figure shows the breakdown voltages and the on-resistance are 285 V and 3.35×10^{-3} Ωcm^2, respectively. The breakdown voltage and the on-resistances obtained from all samples were in the range of 90-305 V and $1.61\text{-}10.2\times10^{-3}$ Ωcm^2, respectively. We plotted on-resistance versus breakdown voltage for 3C-SiC Schottky diodes as well as the theoretical values of 3C-SiC and Si Schottky diodes in Fig. 4. These results indicate that the properties of the SBJs fabricated using homoepitaxially grown 3C-SiC exceed the theoretical limit of Si diodes, though still behind the theoretical limit of 3C-SiC.

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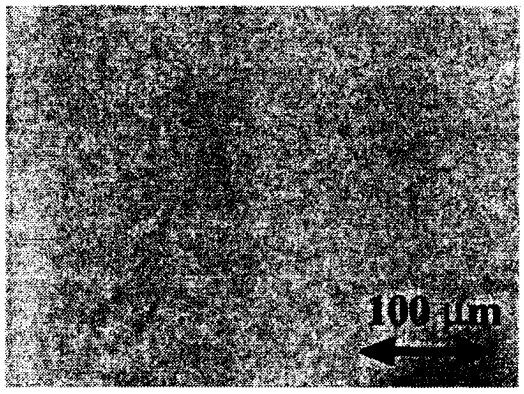

Fig.1 NDIC image of the surface.

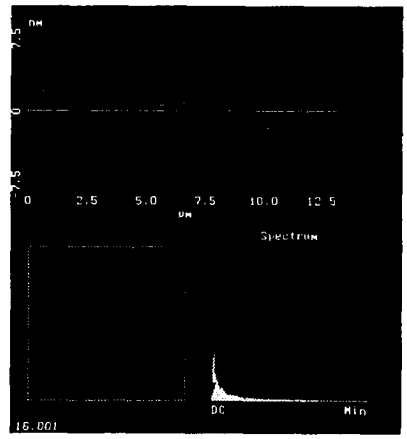

Fig. 2 AFM image of the surface.

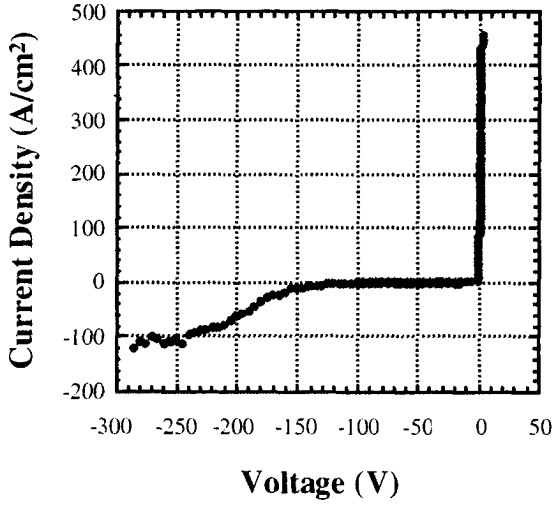

Fig. 3 I-V characterics of SBD on homoepilayer.

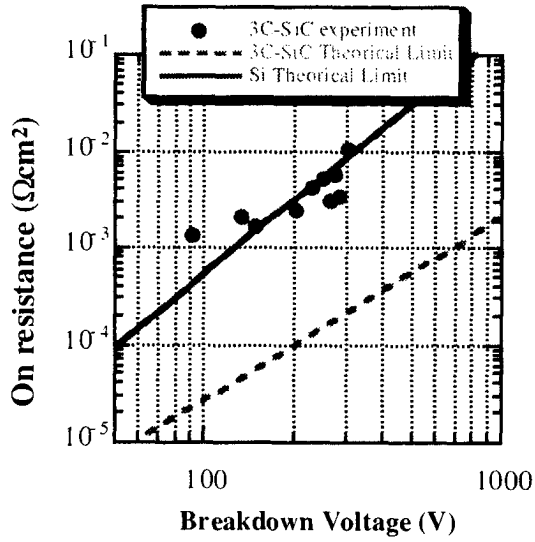

Fig. 4 On resistance versus breakdown voltage.

Void-free epitaxial growth of cubic SiC crystallites during CO heat treatment of oxidized silicon.

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Cubic SiC can be grown epitaxially on single-crystalline silicon substrates by, e.g., chemical vapor deposition (CVD)[1-6]. The first step of the 3C-SiC growth process on Si is the carbonization of the silicon surface to produce seeds for epitaxial growth [7]. Unfortunately the formation of regular shaped voids at the SiC/Si interface below the seeds greatly hinders the development of this technique. It has been shown that C^+ implantation at high temperature (1000-1100 °C) through a protective oxide layer produces epitaxially oriented SiC seeds at the interface, with better quality than those formed in the first stage of the CVD process [2]. The improved quality was explained by the slow growth rate of SiC due to the low carbon ion density. The driving force for diffusion was attributed to the presence of dangling and strained bonds, facilitating the formation of SiC at the interface. Indeed, SiC islands were also formed within the SiO_2 layer with inhomogeneous distribution.

In the present paper we show that annealing a SiO_2/Si structure in CO containing gas without disturbing the SiO_2 layer leads to the diffusion of carbon through the oxide and the segregation of carbon in form of SiC crystallites solely at the interface. These crystals are in epitaxial orientation with the Si substrate and free of voids at their interface. Thereby, the annealing in CO constitutes a new simple process [8] to produce high quality epitaxial SiC seeds on Si.

Experiments performed before the submission of this abstract resulted in square shaped SiC crystallites growing into the Si (001) surface with sizes up to 100 x 100 x 30 nm. The density is 2 x 10^9 cm^{-2} (20 % coverage) and the size distribution is uniform. According to TEM, about 90 % of the crystallites are in perfect epitaxial orientation with the substrate. Grain boundary – free coalescence of crystallites were also observed. The dangling bond density introduced to the interface by the SiC crystallites has been measured by the C-V method in view of possible electrluminescent applications.

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[8] Patent pending

Heteroepitaxy of cubic-SiC (3C-SiC) on Si(100) using porous Si as a compliant seed crystal

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The desirable integration of established and cost effective Si technology with SiC to generate a new family of bandgap engineered, high frequency, medium to high power, high temperature and radiation hard devices has been constantly challenged by the large lattice mismatch between Si and SiC (~ 20%), which has led to difficulties in achieving device-quality materials and interfaces. In this work, a new approach has been implemented to minimize the effects of interfacial strain on the grown layers. Porous Si was used as a compliant single-crystalline elastic seed for growth of 3C-SiC. The growth was then conducted using two methods. In the first, a single gas-source non-toxic trimethylsilane [$(CH_3)_3SiH$] was used for growth of epitaxial 3C-SiC. The method is environmentally friendly and is economical due to the low cost of trimethylsilane (TMS) and Si wafers. In the second, conversion of the porous Si layer into SiC was attempted using high-temperature annealing in methane. However, the latter process did not lead to total conversion of the porous layer. The porous-Si layers were made using anodization of p-type Si(100) wafers in a mixture of hydrofluoric acid (HF) and ethanol in which the anodization current, time, and HF concentration were used to control the porosity and thickness of the porous layer. SiC was grown in a UHV system that was converted into a low-pressure CVD reactor and was fitted with a resistive heating stage capable of heating the samples up to 1200 ^{o}C. The formation of stoichiometric SiC was confirmed by secondary ion mass-spectrometry (SIMS) and Fourier transform infrared spectroscopy (FTIR) while the crystal structure was examined by transmission electron microscopy (TEM) and X-ray diffraction. FTIR showed a strong peak at 800 cm^{-1}, which corresponds to the Si-C vibrational mode. Figure 1 shows a comparison between four samples demonstrating the effects of growth conditions. The intensity of the peak at 800 cm^{-1} is mainly related to the thickness of the sample while the multiple lines within the peak are an artifact of the software used by the BioRad FTIR unit. Sample 28b was grown using conversion in methane atmosphere. The

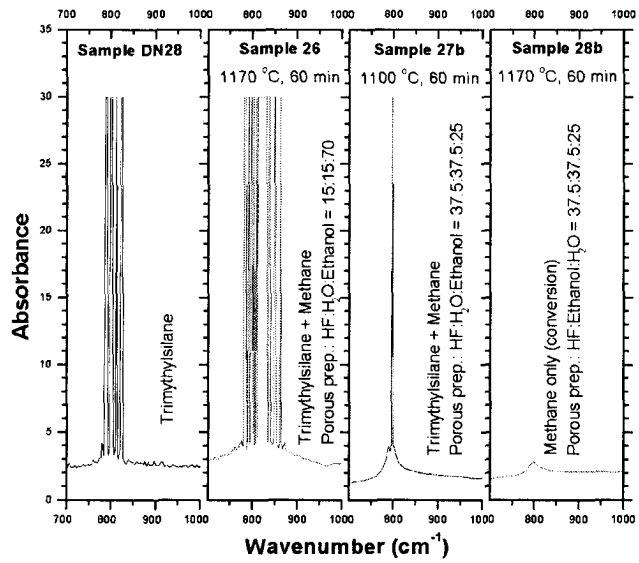

Figure 1. FTIR spectroscopy showing the dependence on growth conditions (see text).

Si-C signal is very small compared to sample 26, which was grown using a mixture of TMS and methane at the same growth temperature and for the same time. This is understandable since the C-H bonding energy in methane is larger than Si-C in TMS resulting in a higher rate of TMS dissociation at a given temperature. In addition, TMS provides both Si and C for growth, while conversion using methane is limited by diffusion of C through the newly formed SiC. The effect of growth temperature is demonstrated in the difference between sample 26 and 27b. Growth using only TMS is essentially similar to growth from a mixture of methane and TMS as shown in the example of sample DN28. Atomic force microscopy (AFM) showed the formation of rough surfaces for thin SiC layers and large flat terraces for thick SiC layers. SIMS analysis showed that the layers were stoichiometric TEM selected area diffraction indicates the formation of fully relaxed single crystalline 3C-SiC(100) on Si(100) wafers (see Figure 2). In some samples, weak spotty rings also appeared in the diffraction pattern indicating the presence of small domains of other orientations. These domains are mainly due to faulty growth within the porous layer resulting from incomplete desorption of oxide from the porous Si layer prior to deposition of SiC. Large area X-ray diffraction shows the domination of SiC(100) peaks but also suggests the presence of a minute amount of SiC(111) and SiC(022).

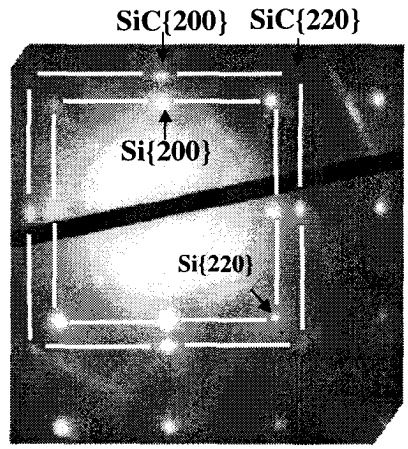

Figure 2.
Selected area diffraction from single crystalline 3C-SiC grown on porous Si substrate. The diffraction pattern represents fully relaxed Si(100) and SiC(100).

The heterojunction Si/SiC was further examined by fabricating heterojunction diodes using Ni as the metal contact to SiC and Al to the p-type Si substrate. Figure 3 shows typical I-V curve obtained from such a device. The insert shows the details of I-V curve near the origin. A record breakdown voltage of ~375V was obtained, which is, up to our knowledge, more than three times higher the highest recorded value in the literature. A high leakage current was associated with most of the heterojunction diodes. This is most likely due to leakage and tunneling through the porous interface.

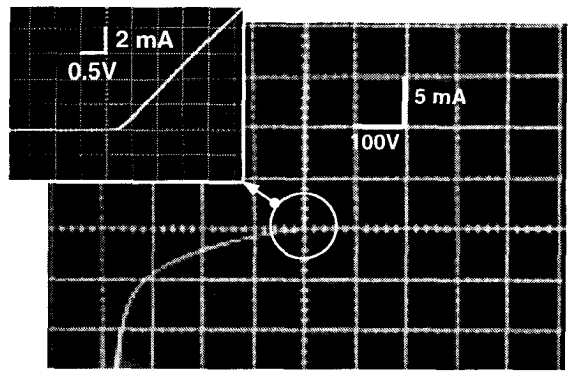

Figure 3. I-V behavior of 3C-SiC/Si(100) heterojunction diode showing a breakdown voltage of ~ 375 V, the highest reported value so far. The insert details the I-V curve near the (0,0) point

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